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11/23/18

CPE 142

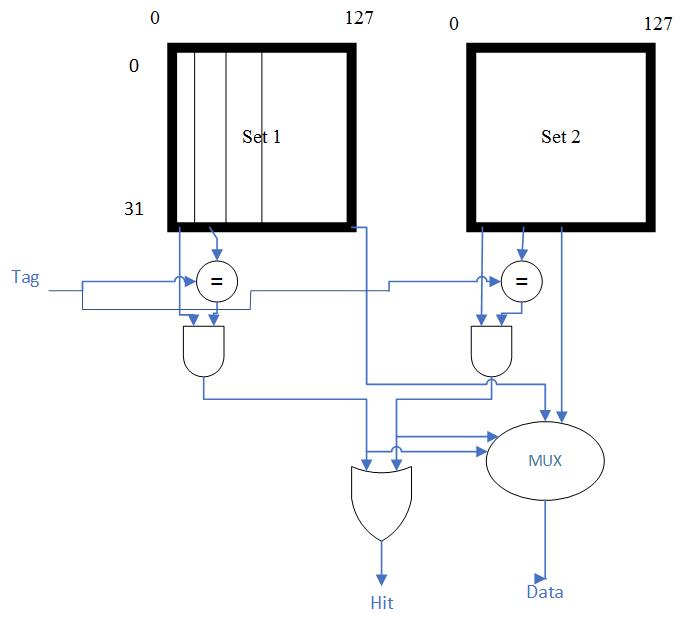
**Assignment 6:**

1. 4.16.1.) Always taken accuracy would be 3/5 or about an accuracy rating of %60. Always not taken would have an accuracy of 2/5 or an accuracy rating of %40. This is done with the branch (T,NT,T,T,NT).

4.16.2.) Accuracy is 0 since it miss predicts the branch to be taken every time since we start in the predict not taken node in the 4th position.

**2.)** Loop Unrolling and Dynamic Scheduling

**3.)** Data design of two way set associative cache.



**4.)**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Address | Hit/Miss | Block 0 | Block 1 | Block 2 | Block 3 | Block 4 | Block 5 | Block 6 | Block 7 |
| 2 | Miss | Mem[2] |  |  |  |  |  |  |  |
| 3 | Miss | Mem[2] | Mem[3] |  |  |  |  |  |  |
| 11 | Miss | Mem[2] | Mem[3] | Mem[11] |  |  |  |  |  |
| 16 | Miss | Mem[2] | Mem[3] | Mem[11] | Mem[16] |  |  |  |  |
| 21 | Miss | Mem[2] | Mem[3] | Mem[11] | Mem[16] | Mem[21] |  |  |  |
| 13 | Miss | Mem[2] | Mem[3] | Mem[11] | Mem[16] | Mem[21] | Mem[13] |  |  |
| 64 | Miss | Mem[2] | Mem[3] | Mem[11] | Mem[16] | Mem[21] | Mem[13] | Mem[64] |  |
| 48 | Miss | Mem[2] | Mem[3] | Mem[11] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 19 | Miss | Mem[19] | Mem[3] | Mem[11] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 11 | Hit | Mem[19] | Mem[3] | Mem[11] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 3 | Hit | Mem[19] | Mem[3] | Mem[11] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 32 | Miss | Mem[32] | Mem[3] | Mem[11] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 22 | Miss | Mem[32] | Mem[3] | Mem[22] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 4 | Miss | Mem[32] | Mem[4] | Mem[22] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 27 | Miss | Mem[27] | Mem[4] | Mem[22] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 6 | Miss | Mem[27] | Mem[4] | Mem[6] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |
| 11 | Miss | Mem[27] | Mem[11] | Mem[6] | Mem[16] | Mem[21] | Mem[13] | Mem[64] | Mem[48] |

**5.)** Fully Associative Cache only contains 1 set

**6.)** 2 to the power n where 2^n is determined by dividing the memory size by the cache size, this is how many blocks we must be able to support in a directly mapped cache.

**7.)** Main memory/cache size then this is divided 4 ways since there are now 4 sets in the associative cache. Each set will be holding an equal number of blocks.

**8.)**